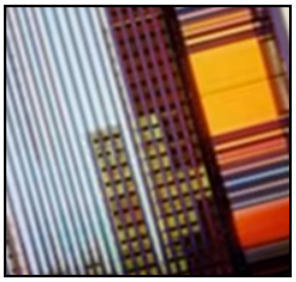
H.264 AVC / MPEG-2 Entropy Encoder IP Block - SNUG (Slice NAL Unit Generator)

IP Description



The SNUG is an entropy encoder and (optional) associated DMA engines that reads swathes of macroblock coefficients and information from memory and writes an encoded bit stream to a circular memory buffer.

H.264 AVC capability

The H.264 standard does not formally define profiles or levels as a way to describe encoders, since these terms refer to the characteristics of a bitstream and the capability of a decoder implementation. However, broadly speaking, the SNUG is capable of encoding bitstreams conforming to the Main, High and High 4:2:2 profiles:

The SNUG does not support the encoding of bitstreams conforming to the Baseline, Extended, and High 10 profiles, and does not support any scalable coding profiles. The SNUG is capable of producing both CAVLC and CABAC bitstreams and supports the production of byte streams conforming to Annex B of H.264.

Restrictions on H.264 syntax and semantics

- The SNUG is designed to support a simple raster scan ordering of macroblocks in which a slice encompasses a number of whole rows of macroblocks.
- The SNUG restricts the luma and chroma samples to have the same depth as one another.
- The SNUG supports reference picture indexes in the range zero to fourteen.
- PCM is not supported.
- Macroblock adaptive frame-field coding (MBAFF) is not supported when the entropy in CAVLC mode. MBAFF is supported in CABAC mode.

H.264 performance levels

Assuming a clock rate of 500MHz or greater SNUG supports level 4.2, and all lower levels, of the Main, High and High 4:2:2 profiles (i.e. 1920x1080x60P). The SNUG itself is capable of supporting bit-rates up to roughly 250Mbit/s, although this is highly dependent on factors outside the control of the SNUG. (For example, if all transform coefficients were zero then the bit-rate would be very low, and limited by the input DMA.)

MPEG-2 capability

The MPEG-2 video standard does not formally define profiles or levels as a way to describe encoders, since these terms refer to the characteristics of a bitstream and the capability of a decoder implementation. However, broadly speaking, the SNUG is capable of encoding bitstreams conforming to Main and 4:2:2 profiles:

Restrictions on MPEG-2 syntax and semantics

The SNUG does not support:

- Encoding of MPEG-1 video bitstreams. (This may have been expected since a compliant MPEG-2 decoder is required to decode MPEG-1 bitstreams)
- Simple Profile.
- Multiple slices in a row of macroblocks.
- Encoding pictures whose vertical size is greater than 2800 lines.
- Encoding of concealment motion vectors.
- Dual Prime motion vectors.

MPEG-2 performance levels

Assuming a clock rate of 500MHz or greater SNUG supports the High level, and all lower levels, of the Main, High, and 4:2:2 profiles (i.e. broadly 1920x1080x30). The SNUG also supports coding at up to twice the pixel rate required of High Level (i.e. broadly 1920x1080x60 – there is no MPEG-2 Level defined to describe this capability). The SNUG itself is capable of supporting MPEG-2 at bit-rates up to roughly 250Mbit/s, although this is highly dependent on factors outside the control of the SNUG. In addition, in a system the performance will be lower because memory accesses are unlikely to be serviced immediately due to contention with other memory clients.

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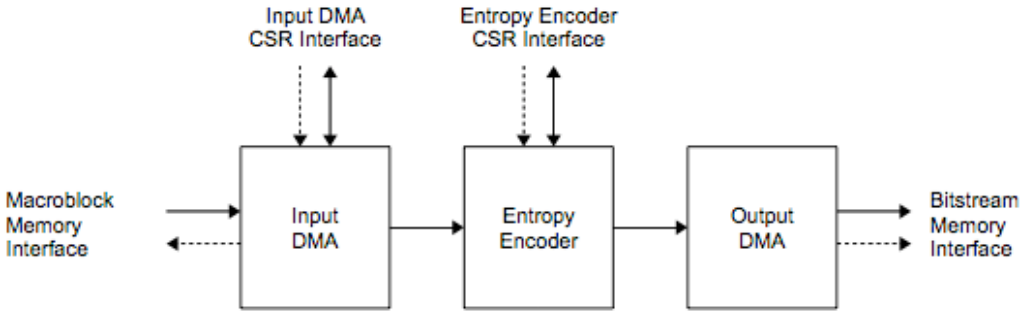
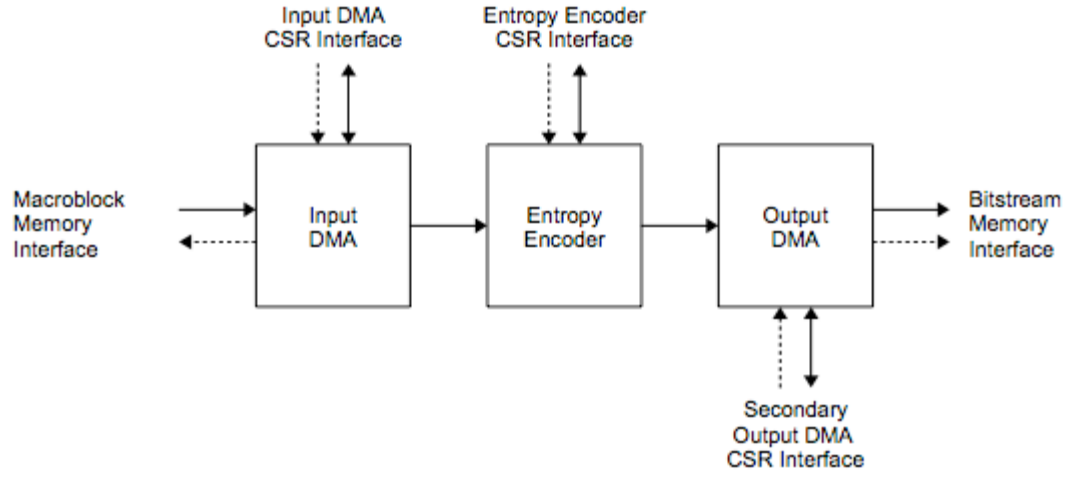
Architecture

The SNUG may be configured at build time in one of two forms. The following diagram illustrates the architecture of the SNUG built for the “synchronous” bitstream writing model:



The SNUG is comprised of an input DMA controller, which reads unencoded macroblock information from one memory interface, an entropy encoder, which encodes the macroblock information to produce a bitstream, and an output DMA controller, which writes the bitstream to a circular buffer via a second memory interface. The input DMA and entropy encoder blocks in the SNUG are provided with a Control and Status Register (CSR) interface that allows an external controller, usually a processor, to configure the block and interrogate current status.

The following diagram illustrates the architecture of the SNUG built for the “asynchronous” bitstream writing model:



When built for the asynchronous bitstream writing model, the output DMA controller is also provided with a CSR interface. This interface is called the “secondary CSR interface” and allows a second controller access to a pair of specialised message queues. A status queue allows the processor connected to the secondary CSR interface access to information as to how much data has been written by the output DMA controller to the output buffer as well as various sideband and metadata information associated with the current slice, that was originally written to the entropy encoder configuration registers via the entropy encoder CSR interface. A stream size queue allows the processor connected to the secondary CSR interface to return information about the total size of the stream to the processor connected to the entropy encoder CSR interface.

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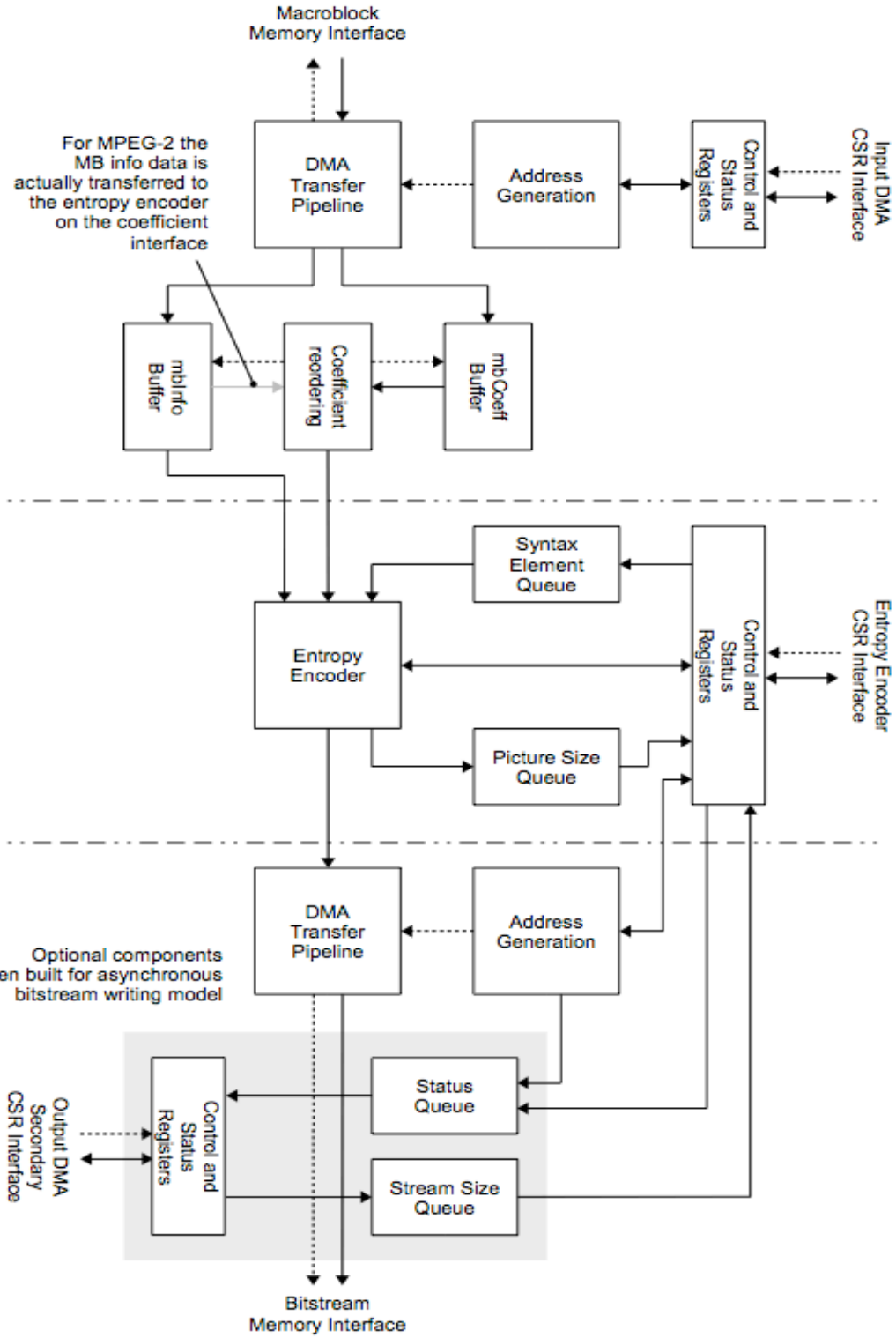

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Notes on area & Power

The entropy encoder can be supplied on its own without the input and output DMA engines.

The following information is for Entropy Encoder block, excluding the DMA engines.

Instance	Cells	Cell Area
ee_top	50117	196353

The area measure (~0.2mm2) is the raw cell area. This should be uplifted by 1/0.8 - assuming 80% routing density.

The RAM requirement is for a total area of 0.3mm2.

Instance	Cells	Leakage Power(mW)	Dynamic Power(mW)	Total Power(mW)
ee_top	50117	0.958	12.214	13.172

The power is for WCCOM (Worst Case Commercial) which corresponds to SS/0.9V/125C (slow, low-voltage, hot).

Dynamic power can be expected to scale up by 12.214mW * (target_voltage/0.9)^2.

Deliverables

- Synthesized Verilog Netlist (TSMC 65nm GP process or equivalent)
- Bit accurate reference C model
- Testbenches
- Specification
- Integration Guide documents